AMENDMENTS TO THE DRAWINGS:

In the Office Action at page 2, the Examiner objected to the drawings. In order to overcome these objections, a replacement figure is submitted herewith. In FIG. 6, the primary crystal grain boundaries are shown inclined to a current direction between active channel regions of the thin film transistor at an angle of $-45° \leq \Theta \leq 45°$. Approval of these changes to the Drawings is respectfully requested.

REMARKS

I. STATUS OF THE CLAIMS

Claims 1-12 are pending in the present application. Claims 1 and 7 are the independent claims.

None of the claims have been amended.

II. THE DRAWINGS

In the Office Action at page 2, the Examiner objected to the drawings. In order to overcome these objections, a replacement figure is submitted herewith.

III. THE REJECTION OF CLAIMS 1, 2, 4, 7, 8, AND 10 UNDER 35 U.S.C. §102(e) AS BEING ANTICIPATED BY ISOBE ET AL. (U.S. PAT. 6,890,840)

Applicants respectfully traverse this rejection for at least the following reasons.

Independent claim 1, recites, amongst other novel features, a thin film transistor (TFT) comprising a lightly doped drain (LDD) region or offset region, wherein the thin film transistor is formed so that **primary crystal grain boundaries** of a polysilicon substrate are not positioned in the LDD or offset region.

Isobe discloses a technique of crystallizing a semiconductor film having an amorphous structure. The semiconductor film is formed by selectively irradiating light onto an amorphous semiconductor film. After cleaning the semiconductor film, an oxide film is formed thereon and a metallic element is added next, forming a thin metallic film (column 5, lines 25-35). The obtained crystalline semiconductor film 106 is patterned to from a semiconductor layer 107. It is possible to lower the concentration of the metallic element within the TFT formation region 302, the channel formation region 303, and the LDD forming region 304 by not including the laser irradiated region 301. Furthermore, the TFT formation region or the channel formation region can be formed by only a crystal aggregate (domain) (column 5, lines 39-56). Accordingly, although Isobe discloses a method for forming a TFT and crystal aggregates, the method disclosed by Isobe is an MILC method. It is well known in the art that with the MILC method, primary crystal grain boundaries cannot be formed and therefore, Isobe fails to anticipate all the features recited in independent claim 1.

Accordingly, Isobe fails to teach or suggest that the thin film transistor is formed so that **primary crystal grain boundaries** of a polysilicon substrate are not positioned in the LDD or offset region.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 102(e) should be withdrawn because Isobe fails to teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that dependent claims 2 and 4 are allowable at least because of their dependence from claim 1, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 2 and 4 also distinguish over the prior art.

Independent claim 7 recites a flat panel display device comprising, amongst other novel features, a thin film transistor formed so that **primary crystal grain boundaries** of a polysilicon substrate are **not positioned in** the **LDD or offset region**.

As noted above, Isobe discloses a crystallization technique for forming crystal aggregates, by using an MILC method, and as noted above it is well known that through this method primary crystal grain boundaries cannot be formed.

Accordingly, Applicants respectfully assert that the rejection of claim 7 under 35 U.S.C. § 102(e) should be withdrawn because Isobe fails to teach or suggest each feature of independent claim 7.

Furthermore, Applicants respectfully assert that dependent claims 8 and 10 are allowable at least because of their dependence from claim 7, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 8 and 10 also distinguish over the prior art.

IV. THE REJECTION OF CLAIMS 1-12 UNDER 35 U.S.C. §103(a) AS BEING UNPATENTABLE OVER ZHANG ET AL. (U.S. PAT. 5,563,426) IN VIEW OF SUZUKI ET AL. (U.S. PAT. 6,274,888).

Applicants respectfully traverse this rejection for at least the following reasons.

Independent claim 1 recites a thin film transistor (TFT) comprising, amongst other novel features, primary crystal grain boundaries of a polysilicon substrate not positioned in the LDD or

offset region.

Zhang discloses a method of manufacturing a TFT using a crystal silicon film obtained by crystallizing an amorphous silicon film using a plurality of island nickel films (column 11, lines 21-22). The TFT includes island nickel regions 2, portions 3, inter-crystalline boundaries 4, an intermediate region 5, a semiconductor region 6 and a gate wire 7 (column 12, lines 25-55; FIGS. 1A-1C). Accordingly, Zhang discloses a method for forming crystal aggregates using an MILC method, and as noted above, this method cannot form primary crystal grain boundaries.

Accordingly, Zhang fails to teach or suggest that the thin film transistor if formed so that **primary crystal grain boundaries** are not positioned in the LDD or offset region, as recited in independent claim 1.

Suzuki discloses a semiconductor device having a thin film transistor having source and drain regions 6 and 7 which can employ LDD (Lightly Doped Drain) structure comprising a lightly doped region and a heavily doped region or the offset gate structure where the source and the drain regions are offset from the edges of the gate electrode (column 7, lines 31-40: FIG. 1A). The method used by Suzuki for forming crystal aggregates is also an MILC method, and as noted above, this method cannot form primary crystal grain boundaries.

Accordingly, Suzuki fails to teach or suggest that the thin film transistor if formed so that **primary crystal grain boundaries** are not positioned in the LDD or offset region, as recited in independent claim 1.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 103(a) should be withdrawn because neither Zhang nor Suzuki, whether taken singly or combined, teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that dependent claims 2-6 are allowable at least because of their dependence from claim 1, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 2-6 also distinguish over the prior art.

Independent claim 7 recites, a flat panel display device comprising, amongst other novel features, a thin film transistor wherein the thin film transistor is formed so that **primary crystal grain boundaries** of a polysilicon substrate are not positioned in the LDD or offset region.

As noted above, neither Zhang nor Suzuki, whether taken singly or combined teach or

suggest a thin film transistor formed so that **primary crystal grain boundaries** of a polysilicon substrate are not positioned in the LDD or offset region.

Accordingly, Applicants respectfully assert that the rejection of claim 7 under 35 U.S.C. § 103(a) should be withdrawn because neither Zhang nor Suzuki, whether taken singly or combined teach or suggest each feature of independent claim 7.

Furthermore, Applicants respectfully assert that dependent claims 8-12 are allowable at least because of their dependence from claim 7, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 8-12 also distinguish over the prior art.

V. CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding rejections have been overcome and/or rendered moot. And further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding rejections, the application is submitted as being in condition for allowance which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited and possibly concluded by the Examiner contacting the undersigned attorney for a telephone interview to discuss any such remaining issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 503333.

Respectfully submitted,

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Date: 10/13/05

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